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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/551,439	09/29/2005	Shinobu Kato	278942US90PCT	3042

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EXAMINER	
PATEL, ISHWARBHAI B	

ART UNIT	PAPER NUMBER
2841	

NOTIFICATION DATE	DELIVERY MODE
01/26/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/551,439	KATO, SHINOBU	
	Examiner	Art Unit	
	Ishwarbhai B. Patel	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 October 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 4-17* is/are pending in the application.

4a) Of the above claim(s) *7 and 10* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *16* is/are rejected.

7)☒ Claim(s) *1,2,4-6,8,9,11-15 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 September 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/5/09*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Pursuant to further review after receipt of the appeals brief filed on October 19, 2009 and an appeals conference, though the arguments are not persuasive, it has been decided to reopen the prosecution in view of not using a secondary prior art or Case Law in 103 rejections of the claims. PROSECUTION IS HEREBY REOPENED. Detailing a new ground of rejection set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below:

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 2, 4, 5, 6 and 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kanbe (US Patent No. 6,333,857) in view of Figueroa (US Patent Application No. 2002/0085334), Forehand (US Patent No. 5,847,936) and Chakravorty (US Patent No. 6,970,362).

Regarding claim 1, Kanbe in figure 2 discloses a multi-layer printed wiring board comprising: a core substrate (110) having a plurality of through holes (107) therein the through holes in the core substrate being disposed so that a ground through hole and a power through hole adjoin each other (see figure 10);

an interlayer insulating layer (121, figure 8) formed on the core substrate; a conductive layer (101, 106) formed on the interlayer insulating layer; and a plurality of via holes provided in the insulating layer and configured to provide electrical connection between the conductive layer and through holes (see figure).

Kanbe does not disclose a distance between the ground through hole and the power through hole is in a range of 60 to 550 μm.

However, the distance between the adjacent via hole will depend upon various factors, for example, the availability of the space for better routing of the traces to avoid shorting of the adjacent pad on via during operation as well as better routing of the traces, or to control the inductance and capacitance.

Figueroa discloses multiple tier structure and recites distance between the holes in a range of 200-500 microns and further recites that when the pitch between the holes is small, the inductance is small but capacitance is also lower. When the pitch between the holes is large, the capacitance is higher, but the inductance is also higher (page 4, paragraph 0046).

Chakravorty (US Patent No. 6,970,362) in figure 2 discloses structure (55) with power and ground layer and recites via pitch about 150 micron (column 4, line 15-28).

Forehand discloses an optimized routing scheme and recites in the background discussion that spacing between adjacent via will have impact on the routing of the traces (column 1, line 41-50).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the structure of Kanbe with a distance between the ground through hole and the power through hole is in a range of 60 to 550 μm, as taught by Figueroa, Chakravorty and Forehand, in order to facilitate better routing of the traces and to control inductance and capacitance.

Regarding claim 2, the modified board of Kanbe further discloses the ground through hole in the core substrate including two or more ground through holes and the power through hole including two or more power through holes (see figure 2), such that the ground through holes and the power through holes are disposed in a grid formation or in a staggered formation at adjacent positions (see figure 10).

Regarding claim 4, the modified board of Kanbe further discloses the diameter of the ground through hole is 50 to 500 μm and the diameter of the power through hole is 50 to 500 μm ((column 19, line 5-10).

Regarding claim 5, the modified board of Kanbe further discloses at least one through of the ground through holes and the power through holes comprises, two or more through holes in a stack structure through all layers of the multi-layer printed wring board up to outermost layer (see figure 8).

Regarding claim 6, the modified board of Kanbe discloses all the features of the claimed invention including the ground through hole and the power through hole, but does not explicitly disclose any IC chip mounted on the board. However, as disclosed by Forehand, it is old and known in the art to mount chip on the upper surface of a board for necessary interconnection. Mounting a chip on the board will meet the requirement of the via holes below the chip.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to have the modified board of Kanbe with an IC chip on the board, which meets the limitation that the ground through hole and the power through hole will be below chip, as taught by Forehand, in order to have necessary interconnection.

Regarding claim 11, the modified board of Kanbe discloses all the features of the claimed invention but does not disclose a capacitor mounted on the surface thereof. However, mounting additional capacitors on the board is old and known in art to control the noise.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the modified board Kanbe with a capacitor mounted on the surface thereof, in order to control the noise.

Regarding claim 12, the modified board of Kanbe further discloses the core substrate (110) is a multi-layer core substrate composed of three or more layers and including a thick conductive layer as an inner layer (the inner layer of Kanbe is considered as thick), and the conductive layer of each inner layer of the core substrate and the conductive layer of each surface are conductive layer for power layer or conductive layer for grounding (see figure 1 and 2).

Regarding claim 13, the modified board of Kanbe further discloses the core substrate (110) is a multi-layer core substrate composed of three layers and including a thick conductive layer as an inner layer (the inner layer of Kanbe is considered as thick), and the conductive layer of each inner layer of the core substrate is conductive layer for power layer or conductive layer for grounding (see figure 1 and 2) and the conductive layer on the front surface side is composed of signal line (via 107 is connected to signal line, figure 1).

4. Claims 8, 9 and 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kanbe as applied to claims 1 and 12 above, and further in view of Strandberg (US Patent No. 6,323,435).

Regarding claims 8, 9 and 14, Kanbe discloses all the features of the claimed invention as applied to claim 1 but does not disclose the relationship between the conductive layer on the core substrate and on the insulating layer as recited in claims 8, 9 and 14.

However, as disclosed by Strandberg in figure 1, it is known in the art to have the conductive layer formed in the buildup portion thinner than that the layer formed in the core substrate to have high density interconnect.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the conductive layer formed on interlayer insulating resin thinner than that of the layer in the core substrate, meeting the relationship as recited in claim 8, and 14, as taught by Strandberg, in order to have high density interconnect.

Further, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. *In re Aller*, 220 F.2d 454, 456, 105 USPQ 223, 235 (CCCPA 1955).

Regarding claim 15, the modified board of Kanbe further discloses the conductive layer in the inner layer of the core substrate is composed on two or more layers as applied to claim 12 above.

5. Claim17 is rejected under 35 U.S.C. 103(a) as being unpatentable over the modified board of Kanbe as applied to claim 12 above, and further in view of Kambe (US Patent No. 6,323,439).

Regarding claim 17, the modified board of Kanbe discloses all the features of the claimed invention as applied to claim 12 above but does not discloses the core substrate is so constructed that a thick conductive layer is disposed as the inner layer and a thin conductive layer is disposed on the surface side. However, providing a thick conductive layer as an inner layer, as disclosed by Kambe, figure 1, layer 11, will provide better mechanical stability and lower electric loss.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the modified board of Kanbe with a thick conductive layer disposed as the inner layer and a thin conductive layer disposed on the surface side, in order to have better mechanical stability and lower electrical loss.

Allowable Subject Matter

6. Claim 16 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

7. Applicant's arguments with respect to claims have been considered but are moot in view of the new ground(s) / new explanation of the rejection.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Chang (US Patent No. 5,774,340 in figure 2 discloses structure with via pitch about 500 micron (column 3, line 43-60) and further it can be seen that the inner layers 16, 18 are thicker than the outer surface layer (26).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ishwarbhai B. Patel whose telephone number is (571) 272 1933. The examiner can normally be reached on M-F (8:30 - 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jinhee Lee can be reached on (571) 272 1977. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jinhee J Lee/
Supervisory Patent Examiner, Art Unit 2841

/Ishwarbhai B Patel/
Primary Examiner, Art Unit 2841

January 15, 2010